What is claimed is:

1. A method, comprising:

providing at least one buffer in an interface between a chipset and memory modules, said at least one buffer allowing the interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and the at least one buffer, and the second sub-interface is between the at least one buffer and the memory modules; and

configuring said at least one buffer to properly latch the data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other.

2. The method of claim 1, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface.

3. The method of claim 2, wherein an operating voltage level of said first sub-interface is less than 1.0 volt.

4. The method of claim 2, wherein an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

5. The method of claim 1, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at higher frequency than the second sub-interface.

6. The method of claim 5, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

7. The method of claim 6, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

8. The method of claim 1, wherein said at least one buffer are provided on a same memory board as the memory modules corresponding to said at least one buffer.

9. The method of claim 1, wherein said chipset is provided on a motherboard.

10. The method of claim 1, wherein said interface between the chipset and the memory modules is a multidrop bus.

11. The method of claim 1, wherein each of said memory modules includes dynamic random access memory (DRAM).

12. The method of claim 1, wherein each of said memory modules includes double data rate (DDR) DRAM.

13. The method of claim 1, wherein each of said memory modules includes quad data rate (QDR) DRAM.

14. A method, comprising:

providing at least one buffer in an interface between a chipset and memory modules, said at least one buffer allowing the interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and the at least one buffer, and the second sub-interface is between the at least one buffer and the memory modules, said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface, and the first sub-interface is operated at higher frequency than the second sub-interface; and

configuring said at least one buffer to properly latch the data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other.

15. The method of claim 14, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface.

16. The method of claim 14, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at higher frequency than the second sub-interface.

17. A method, comprising:

isolating a memory interface between a chipset and memory modules, where said isolating divides the memory interface into first and second sub-interfaces; and

configuring said first and second sub-interfaces to properly transfer data between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other,

wherein said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface.

18. The method of claim 17, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

19. The method of claim 17, wherein said first sub-interface is operated at twice the frequency of the second sub-interface, and a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

20. A system, comprising:

a memory interface between a chipset and at least one memory module; and

at least one buffer disposed in said memory interface to divide said memory interface into first and second sub-interfaces,

where said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface.

21. The system of claim 20, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

22. The system of claim 20, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

23. The system of claim 22, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.